Customer-Designed Carrier Board for AM57x SOM-based Product
Schematic Checklist

General:

- ☐ Design captured in Altium Designer? Reviewing PDF documents?
- ☐ Recommendations:
  - Block diagram on top sheet?
  - Each sheet has PCA part number noted?
  - Each sheet has schematic revision noted?
  - Sheet titles include descriptive name of board and circuitry?
  - "Not installed" components will have X over symbol in variant schematic
  - Part number / value differences will be noted with distinctive text color / font in variant schematic
  - Off-sheet nets have sheet/zone cross-references?
- ☐ Layout /routing directives have descriptive text in schematic?
- ☐ BOM consolidation: commmon use of parts, especially passives
- ☐ Communications interfaces compare to reference circuits

AM57x PINMUX:

- ☐ PINMUX configuration defined?
- ☐ Peripheral selections compatible with available I/O at SOM-Carrier connector set?
- ☐ Does schematic symbol for SOM connector show the pin name for the selected peripheral function?

Connectors:

Baseboard MXM receptacle:

- ☐ Specify JAE MM70-314 series?
- ☐ Symbol pins and names align with SOM definition?
- ☐ Even numbered pins and E groups on top side; odd numbered pins and E groups on bottom side?
- ☐ E-pins defined as separate pins, not grouped?
- ☐ SOM-specific signals (fixed function, PMIC) reserved on connector pins?
  - FPGA_DONE, USB2_ , UART3_, AUXFAN_EN, PB_RESET#, PMIC_POWERGOOD, PMIC_POWERHOLD, WAKEUP1
- ☐ Provisional jumpers: select 1.8V pull-up, GND or float on PMIC_POWERHOLD (pin E3-7)

- ☐ Power pin directions (source/sink) OK?
  - E1-1 to E1-4, E2-1 to E2-4: +5.0 V **to** SOM (4.0 amp max.)
  - E1-8, E1-9, E2-7, E2-8: FPGA Bank I/O voltage **to** SOM (1.0 amp max per bank)
  - E2-9, E4-2, E4-3: VDD_1V8F (+1.8V) **from** SOM (1.5 amp max.)
  - E3-2, E3-3: PS_3V3 (+3.3V) **from** SOM (1.0 amp max.)

HiRose connector:

- ☐ Symbol pins and names align with SOM definition?
- ☐ Symbol pin numbers agree with SOM symbol (odd/even rows not swapped due to bottom side placement on SOM)?

SOM-specific signals (fixed function, PMIC) reserved on connector pins?

- ☐ SATA1_ , FPGA_GXB_ , FPGA_DXP/N, FPGA_VP/VN_0
- ☐ Provisional jumpers:
  - to GND on AM57-BOOTMODE (pin 73) ?
  - to 1.8V on OTP_VPP (pin 75) ?

Power Distribution / Reset:

- ☐ SOM on-board supplies used to power FPGA I/O Bank(s)?
- ☐ PS_3V3 (+3.3V): if used to power Banks 15 and 34 (~500 mA / bank), do not use to power other devices.
- ☐ VDD_1V8F (+1.8V): if used to power Banks 15 and 34 (~500 mA / bank), limited to 500 mA load.
- ☐ SOM Power off control: software or hardware controlled? (POWERHOLD level, u-boot configuration of DEV_CTRL.DEV_ON)

SOM +5V supply:

- ☐ enabled when carrier board input power is applied
- ☐ meets SOM voltage min/max level specifications?
- ☐ output current limit is less than required by SOM for worst case operation?
- ☐ Does on-board reset circuit meet requirements? (reference DevKit)
- ☐ Carrier board voltage rails not sourced from SOM have on-board power supplies?
- ☐ meet voltage min/max and current limit needs?
- ☐ Other on-board supplies are enabled by PMIC_POWERGOOD from SOM (MXM connector: E3-6)
- ☐ Set on-board supply enable threshold to shut down supply outputs while VIN > (highest VOUT + margin)
- ☐ Provide sufficient bulk and decoupling capacitors per application notes.
- ☐ Tantalum / bulk capacitor voltage ratings are >2x power supply rail voltage
- ☐ SOM Power Monitor included? (recommended during development)

Console UART:

- ☐ 1.8V to 3.3V level shifter on UART3 RX and TX signals, if needed?
- ☐ Using UART-to USB translator, like FTDI FT230XS?
- ☐ Powered by external device (VBUS)?
- ☐ USB connector specified is durable for repeated cable insertion cycles? Resistant to being pulled off of PCB pads?

USB-C 3.0 Hub

Proper connection of SuperSpeed nets:

- ☐ SOM TX pair (HiRose pins 33, 35) to Hub Upstream RX pair; SOM RX pair (HiRose pins 27, 29) to Hub Upstream TX pair
- ☐ Hub Downstream TX pair to USB-C connector TX pair; Hub Downstream RX to USB-C connector RX pair
- ☐ Series capacitors on downstream TX lines from Hub to USB-C connector
- ☐ I2C level shifter: 1.8 to 3.3V logic
- ☐ use appropriate external resistor to divide down VBUS to specified VBUS_DET input voltage level.
- ☐ Net attributes noted for controlled impedence, matched lengths?

USB 2.0 Hub

- ☐ Clean power rails supplying hub device; filtered VBUS to USB connectors
- ☐ Use appropriate external resistor to divide down VBUS to specified VBUS_DET input voltage level.

10/100 Ethernet ports

- ☐ I/O voltage, pullup resistors rail V = +1.8V?
- ☐ PHY adddresses are unique for each device?
- ☐ Magnetics center tap V agrees with magnetic circuit for PHY?
- ☐ Separate circuit and chassis ground points for on-board RJ-45 jack(s)?
- ☐ 1.8V to 3.3V level shifter for RJ45 jack LEDs?

Gigabit Ethernet ports

- ☐ Clean power rails supplying PHY device
- ☐ I/O voltage, pullup resistors rail V = +1.8V?
- ☐ Magnetics center tap voltage and passive component support agrees with magnetic circuit for PHY?
- ☐ 1.8V to 3.3V level shifter for RJ45 jack LEDs?
- ☐ in-line and pull-up resistors on RXD lines from SOM to PHY?
- ☐ PHY adddresses are unique for each device?
- ☐ Net attributes noted for controlled impedence, matched lengths?

HDMI Interface:

Audio Interface:

SATA port:

(micro)SD card:

Wireless (BlueTooth):

Analog Circuits

- ▫ Check power pins on opamps
- ▫ Check inverting/non-inverting inputs on opamps
- ▫ Check for required Vos, Ibias, input impedance, R-R in/out on opamps
- ▫ Check supply voltage range of op amps
- ▫ Any tight tolerance parts marked as such