MitySOM™ Document

Document: MitySOM-QC5430/64905430/6490 Carrier Board Design Guide

Revision: 1.0

Date: Jan 21, 2025

1 Overview

1.1 Fast Facts for Getting Started

Facts	MitySOM-QC5430/6490
Required socket connectors	2x Samtec 200-pin high density array SEAM-20-XX.X-X-10-X
Voltage required	4V DC, USB PD Rev 3.0 or a 3.7V Lithium-ion Battery
QC Serial Peripherals*	10x UART, 10x SPI, 14x I2C, 4x I3C, 2x I2S, 2x PCIe Gen 3, 2x SDC, 1x SoundWire, 1x USV 3.1, 1x USB 2.0
QC Display Peripherals*	1x Display Port, 1x Display Port over USBC, 1x MIPI DSI 4-lane
QC Other Peripherals*	4x MIPI CSI 4-lane
*Peripherals share pins, see QCxxxx datasheet and Appendix for specific pin-multiplexing options	

1.2 Introduction

The MitySOM-QC5430/6490 family of modules are System on Modules (SOMs) designed to be easy to integrate into an end-user embedded system. The modules integrate many crucial elements of an embedded system and do so with an established design framework utilizing a common set of core libraries. End-user design of the application PCB is also intended to be as simple as possible, allowing the PCB designer to concentrate on the custom I/O interfaces – especially analog & mixed-signal – instead of getting distracted with the learning curve of designing a brand new embedded digital system from scratch.

Developers are encouraged to review the MitySOM-QC5430/6490 Development Kit design schematics, available on the Critical Link support site. The Development Kit has been qualified and there is a full software support package already available for the interfaces on the board. Customers interested in the Altium CAD design files for the kit should contact Critical Link for access.

1.4 Links to Important Documents and Information

There are many useful documents and resources available that can be referenced when designing a system with the MitySOM-QC5430/6490 module which are listed below. It is recommended that the information on the TI webpages be reviewed often for updates.

MitySOM-QC5430/6490 Data Sheet	https://www.criticallink.com/wp-content/uploads/MitySOM-QC6490-5430_Datasheet.pdf
MitySOM-QC5430/6490 Support Site	https://support.criticallink.com/redmine/projects/mitysom_qc6490/wiki

2 Connectors

The MitySOM-QC5430/6490 utilizes two 200 pin, Samtec High Density Array SEAF connectors for connectivity with the end user application PCB. These connectors were chosen for their high density, compact size, ease of procurement, signal integrity for high speed signals, and low cost. The High Density Array allows the MitySOM-QC5430/6490 module to lay flat, in parallel with the main PCB with low stack heights ranging from 7mm to 18mm.

3 Electrical Requirements

The following sections describe the various electrical requirements for the MitySOM-QC5430/6490 module.

3.1 Power Supplies

Figure 1 provides an overview of the MitySOM-QC5430/6490 power interfaces. The module takes advantage of three Qualcomm power management ICs (PMICs), which require a 3.7V lithium-ion battery or a USB PD compliant input. The PMICs handle USB PD negotiation, battery charging/discharging as well as generate all on-module supplies needed to power the processor, LPDDR5 memory, and FLASH memory. The SOM supply should be capable of 35W to run the SOM in fully loaded conditions. The PMIC includes a 3.3V buck or boost and a 1.8V LDO output that is connected to the external connectors that may be used for IO and peripherals on the carrier card. Note that the carrier board should draw no more than 2A from the 3.3V rail and no more than 1.5A from the 1.8V rail.

3.1.1 Power Supply Sequencing

The MitySOM-QC5430/6490 handles almost all the power sequencing on SOM with the only exception being any potential baseboard IO supplies. These supplies should not be enabled until the SOM is fully powered on and stable. The 1.8V-SOM (pin F18 on J1) is the last supply to come up and should therefore be used to enable IO supplies on the baseboard.

Utilizing the POW_BTN input to the SOM will allow the processor to initiate a power down sequence that allows the PMICs to shutdown the SOM components (processor, RAM, etc.) as well as the associated peripheral IO on the carrier card in an orderly fashion. By default, the system software will recognize a button press on the POW_BTN as a request to power down the system. When off, another request the POW_BTN will cause the PMICs to initiate a power on sequence to reboot the processor.

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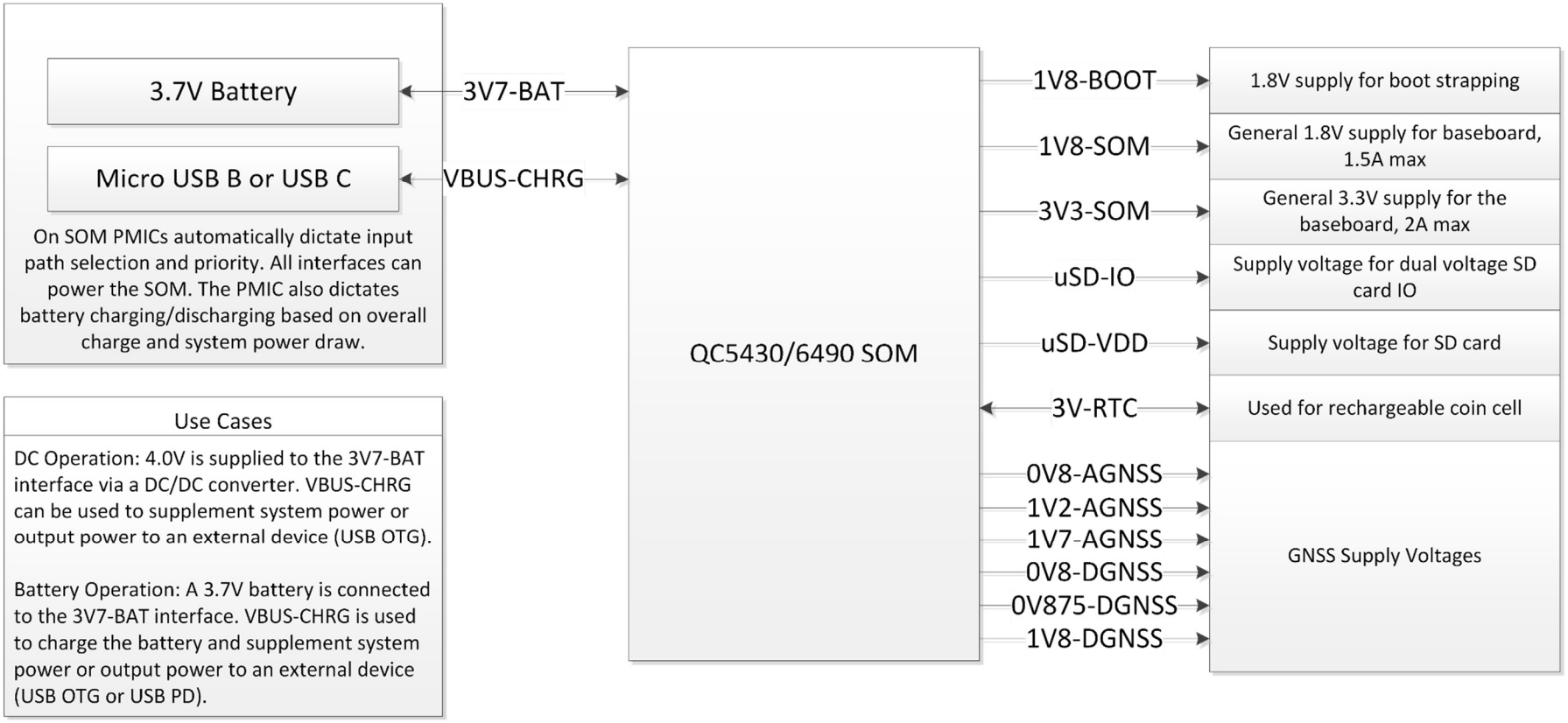

Figure 1 Power interfaces to/from the MitySOM-QC5430/6490

3.2 Recommended Capacitance

The MitySOM-QC5430/6490 module includes some power supply rail bypass capacitors on-board, however additional capacitance is recommended on the carrier board to minimize the ripple effect caused by changing load currents and to be compliant with USB PD standards. It is recommended to place a 1 µF capacitor nearby the main USB VBUS pins in addition to a 40V TVS diode to comply with USB PD and prevent any ESD damage the SOM. The 3V7-BAT should have no capacitance on the baseboard and only a 5V TVS diode to prevent ESD damage to the SOM.

SD and GNSS supplies should have 1uF minimum capacitance on the baseboard.

For RTC support, only the lithium-ion battery should be included close to the SOM. If RTC support is not required, a minimum “keep-alive” capacitance of 10uF should be placed as close to the 3V-RTC pin as possible.

3.3 I/O Interfaces

The I/O pins directly connected to the QC processor can be grouped into the following power domains:

- The USB interfaces – These interfaces utilize low voltage differential signaling input/output in accordance with the USB standard. Data lines should use impedance routing and signal matching should be considered. See Table **1** below.
- MIPI input interface - These interfaces utilize low voltage differential signaling inputs in accordance with the MIPI D-PHY / CSI standard. Data and clock lines should use impedance routing and signal matching should be considered. See Table **1** below.
- MIPI output interface – This interface utilizes low voltage differential signaling outputs in accordance with the MIPI D-PHY / DSI standard. Data and clock lines should use impedance routing and signal matching should be considered. See Table **1** below.
- Display Port interface – This interface utilizes low voltage differential signaling in accordance with the Display Port v1.4 standard. Data lines should use impedance routing and signal matching should be considered. See Table **1** below.
- PCIe interfaces – These interfaces utilize low voltage differential signaling in accordance with PCIe gen 3.0 standard. Data and clock lines should use impedance routing and signal matching should be considered. See Table **1** below.
- QLink interface – This interface utilizes low voltage differential signaling. Data and clock lines should use impedance routing and signal matching should be considered. See Table **1** below.
- SDC interfaces – These interfaces should use impedance routing. See Table **1** below.
- All other QC processor I/O pins – These pins are powered from 1.8 volts on the SOM. Thus only 1.8V logic should be applied to any pins not specified from above.

Signal Group	Impedance	Intra Pair (Pair Matching) (ps)	Inter Pair (Group Matching) (ps)	Max Trace Length (mm)
USB0	90Ω Differential	5	50	150
USB1	90Ω Differential	14	NA	150
MIPI CSIx	85Ω Differential	5	15	130
MIPI DSI	85Ω Differential	5	15	135
DP	85Ω Differential	5	70	NA
PCIe0	90Ω Differential	5	NA	285
PCIe1	90Ω Differential	5	NA	265
QLink	85Ω Differential	10	200	85
SDC1	45Ω Single	NA	42	80
SDC2	45Ω Single	NA	14	36

Table 1 Signal impedance, matching and max trace lengths

3.3.1 I/O Protection

Any I/O interfaces that are external to the MitySOM-QC5430/6490 module must be protected to ensure that no out-of-range voltage conditions occur as all I/O pins are directly connected to the QC processor. The host board should contain the necessary protection/isolation circuits as required to protect the processor. Please refer to the QC Datasheet for details about maximum voltage ranges.

3.4 Module Boot Configuration

The MitySOM-QC5430/6490 is capable of booting from several peripherals as defined by the state of the 4 boot pins at the time of a reset. The state of the 4 data lines B[3..0] is sampled at power-on to determine the search order of peripherals for a valid boot image. All boot signals are pulled down on the SOM via 10kΩ resistors.

The carrier card needs to set B[3..0] during power on reset. If the boot pins are not driven by peripheral IO in the design, a 1kΩ pullup to the 1V8-BOOT on pin J18 of connector J2 can be used to set required boot bits.

The MitySOM-QC5430/6490 provides a force USB boot pin that, if pulled high at the time of boot, will disregard the selected boot setting in favor of booting from the USB0 port.

Care must be taken if the carrier card has peripheral IO that will drive the boot pins. The pins must not be in contention with the intended boot configuration during power on reset

A list of boot peripherals supported by the MitySOM-QC5430/6490 is shown below. The QC processor has provisions to try to boot from set lists of boot interfaces. The processor will attempt to boot from the first listed interface and if no boot configuration is found, will move down the list.

Boot Mode	Boot Media	QC Interface	Can run on Devkit?	Notes
UFS	UFS flash	UFS	Y	
SDC2*	SD Card	SDC2	Y	*Not yet implemented by QC
eMMC*	eMMC flash	SDC1	Y**	*Not yet implemented by QC **Only carrier board with eMMC installed supports this boot media
USB*	External Host	USB0	Y	*Not yet implemented by QC
EDL	Internal	-	Y	Force Boot via USB0

Table 2 Possible Boot Modes, MitySOM-QC5430/6490

Boot Pins [3..1]	Boot Pin [0]	Boot List	Notes
XXX	0	-	Watchdog Enabled
XXX	1	-	Watchdog Disabled
000	X	UFS, SDC2, EDL	
001	X	eMMC, SDC2, EDL	
010	X	SDC2, EDL	
011	X	USB	
110	X	UFS, EDL	
111	X	eMMC, EDL	

Table 3 Common Boot Mode Settings

3.5 Debugger Interface

The MitySOM-QC5430/6490 JTAG/Debugger interface is available on the I/O connector, and it is strongly recommended that this interface be wired up to a header so a debugger can be attached to the design. The Critical Link devkit uses a Samtec FTSH-105-01-L-DV-K-TR header to support the Lauterbach Trace32 MicroTrace for Cortex-M as shown in Figure 2. To enable JTAG communication, PS-HOLD, MODE-0 and MODE-1 must be pulled up to 1.8V. The Critical Link devkit accomplishes this through an optional jumper which can be installed onto a two pin header J25.

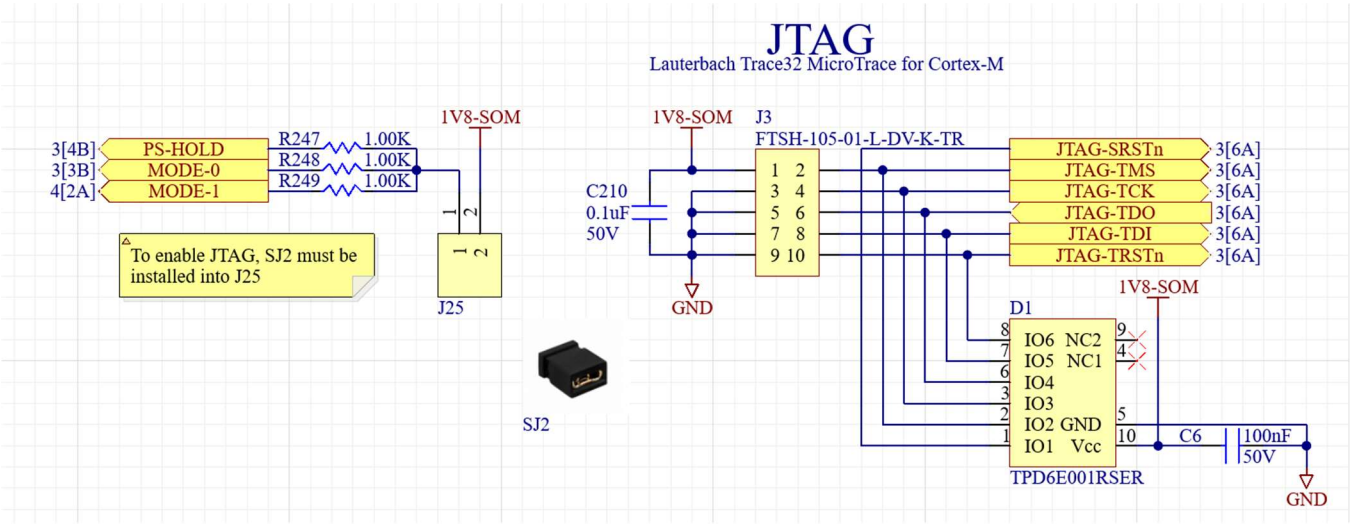

Figure 2: Typical Carrier Card JTAG/Debugger Interface

3.6 RS232 Monitor Interface

It is strongly recommended that GPIO_22 and 23 be used as a general-purpose monitor port. All the u-Boot console and kernel console IO data is routed to that UART (with no HW flow control) by default in the reference software development images. Using these pins for other functions will require modification of low-level boot software (e.g., U-Boot) and the kernel configuration to disable kernel logging to this port. Modern board designs typically use a USB to UART bridge chip to support standard USB style serial ports (COM ports for windows, ttyUSBX ports for Linux). The Critical Link reference design utilizes a FT230XS-U UART to USB bridge chip to interface the UART to support reading text data from the processor.

3.7 LED Power Return

There are two LEDs on the MitySOM-QC5430/6490. The first green LED (D2) is hardwired to a voltage source to indicate that the module is powered while the other RGB LED (D1) is connected to a current source of one of the PMICs and is software controlled.

3.8 USB0 Interface

USB0 is a USB 3.1 interface that supports being powered from USB PD Rev. 3.0 as well as driving DP over USB. If the SOM is instead being powered from the battery interface, USB0 acts as a dual-role port.

In addition to USB data lanes, carrier card designs intending to support DP over USB0 must utilize the USB0-AUX as well as a display port re-driver. Users are encouraged to review the MitySOM-QC5430/6490 development kit as a reference design for DP over USB.

3.9 USB1 Interface

The MitySOM-QC5430/6490 only internally supports being a USB device on this port. The Critical Link devkit is an example of how to use the USB1 interface as a host and users are encouraged to review this reference.

4 Interface Descriptions

4.1 3V7-BAT

This interface is one of the main power lines to/from the MitySOM-QC5430/6490. This interface can support both DC operation, where a constant voltage is supplied to the SOM to mimic a good battery, and also operation from a 3.7V lithium-ion battery. In addition to the 3V7-BAT pins, there are supporting signals that must be used regardless of the required operation. Table 4 summarizes required connections for the battery signals depending on required operation.

Signal	DC Operation	Battery Operation
3V7-BAT	Connect this to a 4V DC regulator to mimic a good battery voltage. Reverse charge protection should be used in between the regulator and the SOM	Connect this to the positive terminal of a 3.7V lithium-ion battery
VBAT-ISNS-P/N	Connect these signals on both sides of a 2mΩ resistor between the regulator and the SOM	Connect these signals on both sides of a 2mΩ resistor between the battery and the SOM
VBAT-SNS-P/N	Connect these signals to the 4V DC regulator and ground as close to the regulator as possible	Connect these signals to the positive and negative battery terminals as close to the battery as possible but after the portection FETs
VBAT-PACK-SNS	Tie to GND	Tie to the negative battery terminal as close to the battery as possible
BATT-THERM	Pull this signal down with a 100kΩ resistor to mimic a good temperature thermistor	Connect this signal to a 100kΩ NTC thermistor that is attached to the battery
BATT-ID	Pull this signal down with a 10kΩ to disable battery charging	Tie this signal to the ID pin of the battery

Table 4 3V7-VBAT signal connections

4.2 USB Interfaces

The MitySOM-QC5430/6490 provides two Universal Serial Bus (USB) interfaces that are mapped directly to the high density array connectors. USB0 can operate in Dual Role mode, is USB 3.1 compliant and can negotiate and recieve USB PD. Dual role mode protocols support dynamic switching from host mode (e.g., for controlling USB mass storage devices such as thumb drives) to device mode (e.g., for interfacing to a PC) based on application software. If USB0 VBUS is connected to the SOM, then the SBU and CC pins should also be connected to the SOM to ensure proper power negotiation between the MitySOM-QC5430/6490 PMIC and power transmitter.

USB1 can operate in device mode, or with supporting circuitry, host mode. This interface is USB 2.0 compliant. If either of the USB interfaces are unused, the signals can be left floating.

4.3 Qualcomm Universal Peripheral (QUP) Ports

The MitySOM-QC5430/6490 provides QUP ports on a large portion of GPIO pins that are able to be muxed to support I2C, SPI, UART and I3C. All GPIOs and GUPs are 1.8V CMOS logic. The QUPs are split into three sections; QUP0 and QUP1 are part of the main processor while QUPIO is on the processor low power island. All three sections of the QUP are split into various channels each with at least 4 lanes. Some QUP ports have up to 7 lanes to support SPI channels with up to 4 chip selects. On the Critical Link devkit, QUP ports are denoted as QX-Y-LZ or LQ-Y-LZ where X denotes the QUP section, LQ denotes the LPI section, Y denotes the QUP channel and Z denotes the QUP lane. Table 5 shows the communication protocol each QUP lane is capable of.

Type	Signal	SPI	UART	I2C	I3C*
Generic I/O	**QX-Y-L0**	MISO	CTS	SDA	SDA
	QX-Y-L1	MOSI	RFR	SCL	SCL
	QX-Y-L2	SCLK	TX	-	-
	QX-Y-L3	CS0	RX	-	-
	QX-Y-L4	CS1	-	-	-
	QX-Y-L5	CS2	-	-	-
	QX-Y-L6	CS3	-	-	-
LPI I/O	**LQ-Y-L0**	MISO	CTS	SDA	SDA
	LQ-Y-L1	MOSI	RFR	SCL	SCL
	LQ-Y-L2	SCLK	TX	-	-
	LQ-Y-L3	CS0	RX	-	-
	LQ-Y-L4	CS1	-	-	-

Table 5 QUP Lane MUX Options

* Only available on Q0-0, Q0-1, Q1-1, LQ-0, & LQ-1

- Can be used as GPIO when communication channel is active

Although a QUP channel can support a communication protocol on some of the lanes and GPIO functionality on the other lanes, a QUP cannot support two different communication protocols within the same channel, even if the lanes don't overlap. For example, even though I2C uses QUP lanes 0 and 1 while UART TX and RX use lanes 2 and 3, both I2C and UART can't be used on the same QUP channel.

Note that not all lanes of QUP channels are pinned out of the MitySOM-QC5430/6490. If these pins are unused, they can be floated or pulled down

4.4 Low Power Island (LPI)

The QC processor supports an internal LPI that allows GPIOs 144-174 to be accessible even if the processor is in sleep mode. These GPIOs also include QUP channels that can be used to continually monitor communication channels and wake up the processor if needed. If these pins are unused, they can be floated or pulled down.

4.5 Emulator/JTAG

The I/O connector on the MitySOM-QC5430/6490 has a full set of JTAG/Debugger signals that can be used to attach an emulator for code downloads and real time debugging. If these signals are not used, they can be left floating.

4.6 Display Controllers

The MitySOM-QC5430/6490 exposes a 4-lane MIPI DSI D-PHY 1.2 interface, a 1.4 Display Port interface, and AUX signals for the USB0 to support Type-C with DisplayPort v1.4. If any of these interfaces are unused they should be floated.

4.7 Secure Digital Card Interfaces

The MitySOM-QC5430/6490 module supports interfacing with up to 2 Secure Digital Card (SDC) format: SDC1, and SDC2. The SDC ports conform to the SD3.0 specifications. If these interfaces are unused they should be floated.

SDC1 is a full 8-bit interface, SDC2 is a 4-bit dual-voltage interface. In general, SDC1 is typically used to interface to an eMMC device and SDC2 is typically used to interface to a MicroSD card as a boot device and/or external storage.

4.8 PCIe

All MitySOM-QC5430/6490 modules support at least the one Peripheral Component Interconnect Express (PCIe) interface. This interface is a Gen 3 1-lane interface. MitySOM-QC5430 with Feature Pack 2 or greater and the MitySOM-QC6490 support a second Gen 3 PCIe interface that is 2-lanes. Both interfaces are root ports. The carrier board should have 0.22uF series DC blocking capacitor by the SOM PCIe RX lines as close to the driving source as possible. The MitySOM-QC5430/6490 has 0.22uF series DC blocking capacitors already on the SOM PCIe TX lines. Note that these capacitors are not included on the Critical Link devkit as PCIe cards generally have the blocking capacitors on the cards. If these interfaces are unused, they should be floated.

5 Mechanical Requirements

The following sections describe some of the mechanical requirements of incorporating a MitySOM-QC5430/6490 module into a board design.

5.1 Module Connectors

The module has two connectors that contain all the power and I/O for the module. The mating connectors are two 200 position Samtec SEAM connectors with PN: SEAM-20-XX.X-L-10 where XX.X denotes the SEAM connectors contribution to the stack height. The Critical Link devkit utilizes SEAM-20-02.0L-10 for a board to board height of 7mm. Taller options of the connectors, e.g., the 8mm or 9.5mm height option, are also suitable.

5.2 Module Clearance – Horizontal Mount

The MitySOM-QC5430/6490 module is positioned in parallel with the carrier board, and as such there is limited clearance between the module and the carrier board. It is not possible to place high-profile carrier board components underneath the MitySOM-QC5430/6490 module. The only components on the bottom side of the SOM are the connectors and therefore components less than 7mm in stack height can be placed in between the SOM and the carrier although components that generate significant heat should are discouraged from being placed under the SOM. Note that as this is based on the 02.0 SEAM connector, if a taller connector is used, more clearance can be obtained under the SOM. The STEP model of the SOM is available from the Critical Link support site, and users are encouraged to verify clearance if making use of the space under the module.

5.3 Mounting Methods

The modules feature an additional optional mechanical attachment method. A hard mechanical attachment by board-to-board standoff or PEM and screw hardware may be used to mount the module. All four corners of the SOM feature a 2.5mm diameter mounting hole that is compatible with M2 size mounting hardware. For details and dimensions of corresponding mounting hole placement on your carrier board please reference Section 6.5 of this document.

Error! Reference source not found. shows the hardware and part numbers utilized by the MitySOM-QC5430/6490 Development kit. The Development Kit carrier card utilizes a 7mm PEM surface mount standoff.

Item	Description	Manufacturer	Part Number
1	RND STANDOFF M2.5X0.45 STEEL 7MM	Würth Elektronik	9774070151R
2	Zinc-plated M2.5 Pan head Screw, 4mm	McMaster Carr	94209A346

Table 6: Optional Mounting hardware used in Development Kit

5.4 Shock and Vibration

For customers who are interested in using MitySOM-QC5430/6490 modules in rugged environments, the optional mechanical attachment methods discussed in section 5.3 enable MitySOM-QC5430/6490 modules to tolerate much greater mechanical shock and vibration forces than without any additional mounting support.

5.5 Thermal Management

The MitySOM-QC5430/6490 has no specific requirements regarding thermal management. The modules can be operated without heat sinks or air flow, and inside tight enclosures. However, if a module is intended to be used in hot industrial environments, it is advisable to test the device in the enclosure and environment that the module will be used in. In these cases, it may be necessary to either add thermal management to the enclosure or lower the operating temperature specification of the end product. Results from thermal testing and measured power consumption of the SOM in a fixed configuration are provided on the Critical Link support site.

The MitySOM-QC5430/6490 has four on board thermistors for temperature monitoring. RT1 measures the temperature right next to the main SOM PMIC, RT2 measures the heat at the coolest/ambient SOM temperature, RT3 measures the temperature right next to the QC processor and RT4 measure the temperature at the UFS.

The carrier board should have a 100kΩ NTC thermistor placed at the USB connector and tied to USB0-THERM on connector J1 pin B16 and GND. This allows the PMIC to monitor temperature rise at this connector and throttle input power depending on the temperature rise.

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6 Board Layout Recommendations

The following sections discuss topics for successful board layouts incorporating the MitySOM-QC5430/6490 module.

6.1 Placement

Placement of the module site is crucial to a successful carrier board layout. Because the module connector footprints are fine-pitch and high density, it is generally best to place the connectors fairly centered in the overall board layout. This placement allows traces to be routed out from all sides of the connectors. The use of fewer signal layers, and therefore fewer vias, generally results in a more compact design with better signal integrity than a board using many layers and vias.

6.2 Pin-out and Routing

Care must be taken when routing the MitySOM-QC5430/6490 high speed interfaces – specifically the USB 3.1 port, the MIPI CSI ports the MIPI DSI ports, the PCIe ports and the QLink ports. Please refer to Table 1 for guidance related to these pins. In general, it is a good idea to route the outer layers of pins out from the connectors on L1, the next inner rows should be taken down into the PCB and routed out on the next signal layer, and so on.

6.3 Access Issues

Given that it is possible and often desirable to make best use of available space by placing components underneath the MitySOM-QC5430/6490 module (refer to section 5.2), hardware and software engineers who will be debugging code on the platform could find themselves in a tough situation if the component they need to access is blocked by the installed MitySOM-QC5430/6490 module. Because of these situations it is advisable to either not use the space under the MitySOM-QC5430/6490 module for active components that might need live probing with the MitySOM-QC5430/6490 in-circuit, or only place circuits there that are already tried and tested by engineers on other platforms. If an obscured circuit does need to be probed, it may be necessary to solder temporary wires onto probe points. If an unverified circuit is placed under the SOM, make debugging easier by designing the board with bottom-side test points, if this is possible on a given design.

6.4 PCB/PCA Technology

The MitySOM-QC5430/6490 module does not have any specific requirements about the PCB technology used for its carrier board. The required socket connectors are available as RoHS compliant and may be used in both leaded and lead-free assembly processes. One recommendation is to fabricate the carrier board thick enough to rigidly support the MitySOM-QC5430/6490 socket connector. In practice, FR-4 with a common finished thickness of 0.062 inches is enough for all types of MitySOM-QC5430/6490 modules. Another recommendation is to use via in pads that are filled and capped to make break out routing easier on the connector layer.

6.5 PCB Footprints

The recommended PCB footprint for the Samtec SEAM-20-02.0-L-10-1-A-K-TR series connector can be found on the Samtec website. Additionally, Samtec offers a download of the footprint that can be imported into common design suites. Figure 3 shows the placement of the connector alignment holes with respect to the center of the SOM mounting holes. Note that J1 denoted below mates with the SOM J1 and J2 mates with the SOM J2.

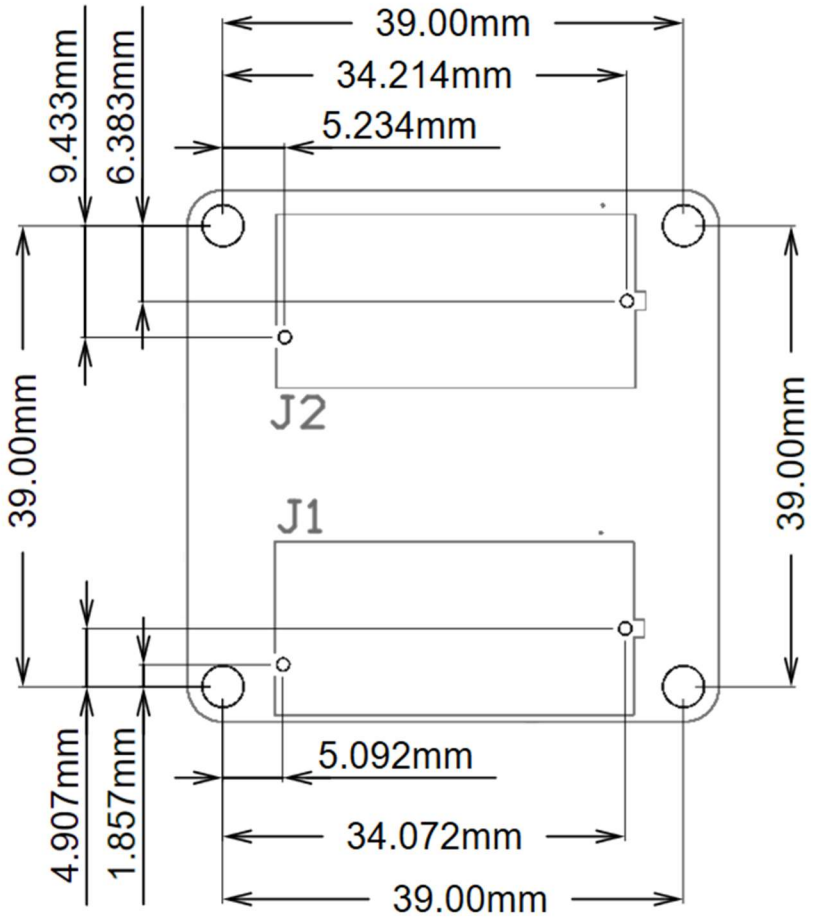

Figure 3: MitySOM-QC5430/6490 Mounting Hole Location

7 Revision History

Revision	Date	Description of Changes
1.0	22-January-2025	Initial Revision